REMARKS

In the Office Action, claims 1-6, 8-19 and 44-46 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent No. 5,633,939 to Kitani et all. ("Kitani"), and claims 50-59 and 72-82 stand rejected under 35 U.S.C. §102(b) as allegedly anticipated by U.S. Patent No. 5,457,811 to Lemson ("Lemson"). Claim 7 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Kitani in view of U.S. Patent No. 4,947,133 to Thomas (Thomas"), claims 20-23, 25 and 26 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Kitani in view of U.S. Patent No. 4,628,526 to Germer ("Germer"), claim 24 stands rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Kitani in view of Germer and further in view of U.S. Patent No. 5,444,788 to Orban ("Orban"), claims 47-49 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Kitani in view of U.S. Patent No. 4,376,916 to Glaberson ("Glaberson"), and claims 60-71 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Lemson. Claims 83-99 are new.

The Office Action also objects to drawings 1a-1e and 2. In the Application, claims 1-26 and 44-82 are pending and claims 27-43 are withdrawn by restriction.

The Objections To The Drawings

In this Amendment, Applicants submit replacement drawings including the amendments requested by the Examiner. Consequently, Applicants request withdrawal of the objections.

The Rejections under 35 U.S.C. § 102(b)

Claim 1 of the present Application requires gain calculate logic responsive to an input signal for calculating a gain calculate signal, and synchronizer logic responsive to the input signal and the gain calculate signal for synchronizing the input signal and the gain calculate signal to provide an output signal. In rejecting claim 1, the Office Action suggests that rectifier 13, comparator 15 and electronic volume controller 18 of Kitani teaches the required gain calculate logic, that the output of Kitani's binary comparator 15 teaches the required gain calculate signal, and that Kitani's counter 16, programmable frequency divider 19, and first volume controller 11 teach the required synchronizer logic responsive to the input signal and the gain calculate signal. Applicants respectfully disagree.

In Kitani, rectifier 13 performs full-wave rectification of an input signal 10 and this rectified signal is then low-pass filtered using filter 14 before being compared to an amplified constant voltage control signal (Kitani at col. 1, lines 38-48). This processing of input signal 10 blocks substantially all AC components to provide a signal representative of the power in the input signal 10 (*see, e.g.*, Fig 9A). As clearly depicted in Figs. 9B and 9C (for example), the output of comparator 15 is a binary, two-state signal used for controlling whether counter 16 counts up or down. Gain in Kitani's compander is described as increasing or decreasing with successive counts and is not limited to two levels (*see* Figs 9B and 9C). Thus, the combination of rectifier 13, low-pass filter 14, comparator 15 and electronic volume controller 18 proposed by the Office Action cannot provide even the gain taught in Kitani. Therefore, the cited signal does not teach a gain calculate signal and the cited combination cannot reasonably be said to teach or suggest the gain calculate logic required in claim 1.

Applicants observe that output of counter 16 sets gain for volume controllers 11 and 18 in Kitani, although the Office Action alleges that counter 16 is part of a group of components that teach synchronizer logic. Nevertheless, Applicants address the allegation that the combination of Kitani's counter 16, programmable frequency divider 19, and volume controller 11 teaches or suggests the synchronizer logic required by claim 1.

The combination proposed in the Office Action does not teach or suggest synchronizing an input signal with any other signal in Kitani's compander. Volume controller 11 is taught as a variable gain amplifier where gain is controlled by counter 16 (Kitani at Figs. 4 and 5 and at col. 6 lines 31-48). As plainly shown in Figs. 9A-9C of Kitani, a change in volume of an input signal causes a change in gain provided by variable gain amplifier 11 such that the changes in gain are slowed and ramped relative to transitions in input signal 10 power. As discussed above, these transitions in input signal power are determined from a signal provided by rectifier 13 and low-pass filter 14 after substantially all frequency components of input signal 10 have been removed. Clearly then, output of comparator 15 and changes in gain are not synchronized to the input signal as required in claim 1.

Applicants note that Kitani's counter 16, programmable frequency divider 19, and volume controller 11 and their respective outputs are explicitly synchronized to an external clock signal rather than the input signal. Kitani teaches a clock pre-scalar 19 and up/down counter 16 that are synchronous to a clock signal "from the outside of the compander circuit" (see Kitani at Figs. 4 and 6, col. 6, lines 18-31 and col. 7, lines 11-19). No other input to

counter 16 is synchronous with the input signal. Up/down control of counter 16 is derived from a low-pass filtered, rectified version of the input signal that is stripped of substantially all but its DC component. Therefore, the output of the up/down counter 16 is synchronous only with the external clock and Kitani cannot be said to teach output of comparator 15 or counter 16 as being synchronous with input signal 10.

Furthermore, Kitani teaches a different purpose for the combination of elements cited in the Office Action. Specifically, Kitani teaches varying attack and recovery times by changing the frequency of the clock signal applied to the up/down counter (Kitani at col. 8, lines 1-32). Such use of the cited combination would require no synchronization with the input signal. Therefore, Applicants respectfully submit that Kitani's clock pre-scalar 19 and up/down counter 16 do not teach or suggest synchronizing the input signal and the gain calculate signal to provide an output signal as required in the claims. For at least these reasons, the rejection of claim 1 should be withdrawn.

Claims 2-4 are allowable for at least the same reasons that claim 1 is allowable. Furthermore, the Office Action bases its rejections of these claims in part on the proposition that a variable gain amplifier 11 including a switchable array of resistors teaches or suggests a gain cell (*see, e.g.*, Figs. 10 and 29A). In asserting that Kitani teaches the required synchronizer block that provides a gain signal and a delayed signal to the gain cell, the Office Action finds a delay logic element in an overflow counter that provides clock control signals to up/down counter 16 (Kitani, Figs 29 A and 32). However, claim 4 requires that in addition to the gain cell receiving both the gain signal and a delayed signal, the output of the gain cell is the output signal. In Kitani, the output of counter 16 – which receives the delayed clocking signal – is not the compander output signal. The overflow counter 131 does not provide any delayed signal to variable gain amplifier 11. The counter 16 does not provide ***both*** a gain signal ***and*** a delayed signal to variable gain amplifier 11 but 16 merely provides a value that is decoded to generate a desired gain in variable gain amplifier 11 (*See, e.g.*, Figs 4, 6, 10, 29A and 32). Therefore, Kitani does not teach providing a gain signal and a delayed signal to the purported gain cell. Applicants respectfully submit that the rejections are improper for at least these additional reasons.

Claims 5 and 6 are allowable for at least the same reasons that claim 1 is allowable. Furthermore, in rejecting these claims, the Office Action relies on the proposition that switching of comparator 15 and counter 6 directional control teaches or suggests detecting a predetermined condition of the input signal. These rejections are ill-founded. Kitani does not

teach detection of a predetermined condition in the input signal. As shown above, the comparator 15 in Kitani compares power level of a *rectified, low-pass filtered version of the input signal* against an amplified constant-level reference voltage. Because of the rectification and filtering, no predetermined condition would be detectable in Kitani which, in any case, teaches no detectors. For example, zero crossings are eliminated by full-wave rectification and consequently, zero crossings in the input signal 10 would be undetectable by comparator 15 (*see* Kitani at col. 1, lines 38-48).

Applicants also note that the Office Action proposes that the output of comparator 15 teaches the required gain calculate signal. Claim 4 requires that the gain calculate signal is generated only after the predetermined condition of the input signal occurs. Comparator 15 has only two possible states (used to set count up or count down) and nothing in Kitani suggests that comparator output is generated only after the predetermined condition of the input signal occurs or how such conditional generation of a binary signal could be accomplished. For at least these additional reasons, the rejections of claims 5 and 6 are improper and should be withdrawn.

Claims 8-19 are allowable for at least the same reasons that claim 1 is allowable. Furthermore, these claims further require monitor logic for monitoring the input signal and power estimator logic responsive to the monitor logic for providing the gain calculate signal. The Office Action offers the Kitani comparator 15 as teaching monitoring logic and low pass filter 14 as a power estimator, even though the teachings of Kitani have comparator 15 receiving a signal from low pass filter 14 – opposite to the order of the claim. Nevertheless, as discussed above, comparator 15 is not capable of monitoring the input signal since it receives a rectified, low-pass filtered representation of the input signal. Therefore, for at least these additional reasons, the rejections of claims 8-19 should be withdrawn.

Regarding claims 44-46, Applicants respectfully submit that the Office Action fails to identify a compander having a signal processing stage including demodulating and filtering. The purported teaching of demodulation in Fig. 19 of Kitani is taught as been separate from the compander in a block diagram of a communications device. Consequently for at least these reasons, the rejections of claims 44-46 should be withdrawn.

The Office Action relies on Lemson in rejecting claims 50-82 and 72-82, alleging that Lemson teaches a comparator. Lemson does not teach a compander. Lemson is directed to a dynamic range enhancing system and a process for increasing the dynamic range of a

transmission link (Lemson at col. 1, lines 14-17). Lemson states an objective of "enhanc[ing] the overall dynamic range of a transmission system without the need for a wideband feedback loop, which is typically required with companders" (Lemson col. 9, lines 29-32). Thus, Lemson does not teach a compander.

Furthermore, Lemson does not teach a first input comprising at least one local power estimator signal and a second input comprising at least one external power estimator signal, as required in the rejected claims. The rejections cite a DC processor 56 and an AC processor 58 taught in Figs. 6 and 6a of Lemson. However, Lemson does not teach that either processor 56 or 58 is an external processor and, to the contrary, teaches that both processor 56 and 58 process the same signal and provide an output to combining unit 60 (Lemson at col. 26, lines 55-61). Therefore, Lemson cannot be construed as teaching or suggesting the required at least one local power estimator signal and at least one external power estimator signal.

Furthermore, Lemson does not teach modulating, scaling, filtering or other processing of external power estimator signals whether internal or external. Although Lemson may discuss such processes, they are not taught in context of processing power estimator signals.

Therefore, for at least these reasons, the rejections of claims 50-59 and 72-82 should be withdrawn.

The Rejections under 35 U.S.C. § 103(a)

Given the foregoing deficiencies of the individual primary and secondary references asserted by the Examiner, Applicants respectfully submit that the claim rejections based upon 35 U.S.C. §103(a) are improper, and that an ordinarily skilled artisan would not have been motivated to combine the references in the manner suggested by the Examiner or to reasonably expect a successful outcome from such combination.

Regarding claim 7, Kitani does not detect zero crossings and the full-wave rectification and low pass filtering of input signal 12 render such detection impossible. Therefore, no motivation could have existed to combine Thomas's detection of "no zero crossing" since no zero crossing would be expected when the rectifier is provided to eliminate zero crossings. Consequently, a skilled artisan would not have been motivated to combine the references and could not have reasonably expected to achieve a successful outcome form such combination. Therefore, the rejection of claim 7 should be withdrawn.

Regarding claims 20-26, the attack and release performance of Kitani is governed by the operation of up/down counter that would be unaffected by Germer's differentiators which

cooperate with a coincidence detector 23 to select a positive or negative voltage – based on whether slopes are different – which is then averaged by a low pass filter. Attack time is taught in Kitani as being controllable through the frequency of the clock signal applied to the up/down counter (Kitani at col. 8, lines 1-12). Thus, the references teach alternative means to affect attack performance and no motivation would have existed to combine the approaches. For at least these reasons, the rejection should be withdrawn.

Regarding claims 47-49, Glaberson does not cure the deficiencies of Lemson discussed above. Additionally, Glaberson does not permit selection between different low-pass filters and requires summation of all signals. For at least these reasons, the rejection should be withdrawn.

Regarding, claims 60-71, as shown above, Lemson does not teach all elements of the independent claim 50 and therefore is not susceptible to rejection for obviousness based on duplicating untaught parts for multiple effects. For at least these reasons, the rejection should be withdrawn.

The Amendments To The Claims

Claim 68 is amended to correct a typographical error. Dependent claims 83-99 are new, add no new subject matter to the Application and further distinguish the claimed inventions from the art of record.

CONCLUSION

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition of allowance and a Notice to that effect is earnestly solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Please charge any fees associated with the submission of this paper to Deposit Account Number 033975. The Commissioner for Patents is also authorized to credit any over payments to the above-referenced Deposit Account.

Respectfully submitted,
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